REMARKS

In the Office Action, Claims 1-22 are pending, were examined and stand rejected. In this Response, Claims 7, 17 and 20 are amended, no claims are cancelled and no claims are added. Applicants respectfully request reconsideration of pending Claims 1-22 in view of the following remarks.

I. Claim Objections

The Examiner rejects Claim 1 because of the following informalities: "An memory controller" should be --A memory controller--.

Accordingly, in view of Applicants' amendment to Claim1, Applicants respectfully request that the Examiner reconsider and withdraw the objection to Claim 1.

II. Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claims 1-22 under 35 U.S.C. §103(a) as being unpatentable over Applicants' admission of prior art ("AAPA") in view of U.S. Patent No. 5,661,751 to Johnson ("Johnson"). Applicants respectfully traverse this rejection.

Regarding Claim 1, Claim 1 recites a memory controller included in the following claim features which are neither taught or suggested by the prior art combination of AAPA in view of Johnson:

> a memory enable deassertion delay (MEDD) logic to set a wait period for the deassertion of a memory enable signal after completion of a memory operation, the wait period chosen for a preferred latency versus power savings tradeoff; and
>
> the memory enable signal used when reading from and writing to the memory. (Emphasis added.)

According to the Examiner:

> AAPA teaches a memory controller comprising a memory enable deassertion logic for deasserting a memory enable signal to the memory [application's specification, p. 1, ll. 6 of pars 0003], the memory enable signal is used for reading and writing operation [application's specification, par. 0002]. (See pp. 2, ¶ 5 of the Office Action mailed 6/7/06.)

Applicants respectfully disagree that the background section of the Applicants' specification discloses a memory controller comprising memory enable deassertion logic for deasserting a memory enable signal to the memory. Applicants respectfully submit that Applicants' background provides no admission regarding a memory controller or any logic of a memory controller for deasserting a memory enable signal to a memory. The background of Applicants' specification describes standby low power modes of a synchronous DRAM memory, which may be controlled according to a Clock Enable (CKE) signal to power up/down the memory to enable/disable access for writing or reading, as suggested by the Examiner. (See supra.)

As correctly noted by the Examiner, AAPA does not teach that the deassertion can be delayed for a period of time after completion of a memory operation. As a result, the Examiner cites Johnson. Johnson discloses a system and technique for power management of a universal asynchronous receiver/transmitter UART by automatic clock gating. As discloses by Johnson:

> A universal asynchronous receiver and transmitter, commonly abbreviated as a UART, is a prevalently employed communications element within computer systems that allows serial data transmission and reception. A major task of a UART is parallel-to-serial and serial-to-parallel conversion. (Col. 1, lines 19-24.) (Emphasis added.)

As further taught by Johnson:

> In addition to the basic serial input and output functions, most UART circuits also include connections for modem control handshake signals for RS-232 operation. Details regarding specific UART circuits may be found in a host of publications of the known prior art. (Col. 1, lines 42-47.) (Emphasis added.)

As know to those skilled in the art of UART circuits, and as indicated by the cited passages above, a UART circuit is the key component of the serial communications subsystem of a computer. Serial transmission is commonly used with modems and for non-network communications between computer, terminals and other devices. Furthermore, the baud rate signal referred to by Johnson (see for example col. 2, lines 59-60) is a measurement of transmission speed in asynchronous communication. Conversely, memory such as the synchronous DRAM memory referred to in the background of Applicants' specification, operates according to a source synchronous protocol. Hence, for at least the reasons provided above,

Applicants respectfully submit that the power management technique of a UART, as taught by Johnson, refers to is analogous art to the memory controller, for example as recited by Claim 1.

As indicated by the Examiner, Johnson discloses:

> Deassertion of the clock enable signal can be delayed by a period of time after completion of an operation (activity detection) [col. 5, lines 46-58], the delay period chosen for a preferred latency versus power savings tradeoff [col. 5, lines 26-30]. (P. 3, ¶ 1 of the Office Action mailed 6/7/06.) (Emphasis added.)

Applicants respectfully disagree with the Examiner's contention that the delay period for deassertion of the clock enable signal after completion of an operation is chosen for a preferred latency versus power savings tradeoff, as recited by Claim 1. According to the Examiner, this teaching of Johnson is provided in column 5, lines 26-30. As indicated by such cited passage:

> When the detected activity later completes and is no longer detected by clock control unit 102, and if none of the other predetermined system activities is currently being detected, the clock control unit 102 deasserts the clock enable signal such that the Clock IN signal at lines 136 is gated. As stated previously, when the Clock IN signal is gated, a baud rate signal is no longer generated at line 124, and power consumption is reduced. (Col. 5, lines 23-30.) (Emphasis added.)

Although the above cited passages refers to the reduction of power consumption, due to deassertion of the clock enable signal, the predetermined delay, as taught by Johnson, is not chosen for a preferred latency versus power savings tradeoff, as recited by Claim 1. Regarding such delay period:

> It is further noted that the deassertion of the clock enable signal by the clock control unit 102 in response to the completion of a detected system activity (as described above) may be delayed by a predetermined amount of time after the system activity completes or is no longer detected. Such a predetermined delay may be desirable to allow the UART 108 to complete operations associated with the detected activity. For example, as stated previously, the clock control unit 102 asserts the clock enable signal when the reset signal becomes inactive, the clock control unit 102 may be configured to wait a predetermined time before deasserting the clock enable signal. This may allow, for example, certain initialization operations to complete. (Col. 5, lines 46-59.) (Emphasis added.)

As indicated by the cited passages above, the predetermined delay is desirable to allow the UART 108 to complete operations associated with the detected activity. As further indicated

by the cited passage above, the waiting of the predetermined time before deasserting of the clock enable signal is provided to allow initialization operation to complete. Applicants respectfully submit that the delaying of deassertion of a clock enable signal by a predetermined amount of time to allow the completion of operation(s) associated with a detected activity or to allow initialization operation to complete fails to teach or suggest the selection of a delay period for preferred latency versus power savings tradeoff. In other words, delaying the deassertion of an enable signal to allow either initialization operations to complete or to allow completion of operations associated with detected activity provides no disclosure, teaching or suggestion with regard to the preferred latency versus power savings tradeoff, as recited by Claim 1.

As mandated by case law, "To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). ("Royka")

Here, the Examiner incorrectly identifies the background of Applicants' specification as teaching a memory controller comprising memory enable deassertion logic. Applicants respectfully submit that the background of Applicants' specification is expressly limited to the description of a synchronous DRAM memory which includes a clock enable (CKE) signal which is used to power up the memory to enable access for writing or reading. Hence, Applicants respectfully submit that AAPA fails to teach or suggest a memory controller comprising memory enable deassertion logic for deasserting a memory enable signal to the memory, as suggested by the Examiner.

Furthermore, Applicants respectfully submit that the Examiner's characterization of Johnson, which discloses a technique for automatic clock gating of a universal asynchronous receiver/transmitter, is completely distinct from the memory controller recited by Claim 1. Moreover, Claim 1 recited that the wait period for the deassertion of the memory enable signal after a completion of a memory operation is chosen for a preferred latency versus power savings tradeoff. Conversely, the predetermined amount of time for delay of the deassertion of the clock enable signal, as taught by Johnson, is provided to enable the completion of operations associated with a detected activity or to allow initialization operation to complete (see col. 5, lines 46-59.)

Accordingly, for at least the reasons provided above, Applicants respectfully submit that the predetermined amount of time referred to by Johnson is not chosen for preferred latency versus power savings tradeoff. Applicants respectfully submit that the entire text of Johnson is devoid of any teaching or suggestion regarding the a preferred latency versus power savings tradeoff for the selection of a wait period for deassertion of a memory enable signal after completion of the memory operation, as recited by Claim 1.

Consequently, Applicants respectfully submit that the Examiner fails to establish a prima facie case of obviousness of Claim 1 since the prior art combination of AAPA in view of Johnson fails to teach or suggest all claim features, as recited by Claim 1. Id.

Therefore, for at least the reasons provided above, Applicants respectfully submit that Claim 1, as well as dependent Claims 2-6, are patentable over the prior art combination of AAPA in view of Johnson. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 1-6.

Regarding Claim 7, Claim 7 recites the following claim features which are neither taught or suggested by the prior art combination of AAPA in view of Johnson:

> setting a variable memory enable signal de-assertion (MEDD) wait time based on a preferred latency versus power savings tradeoff; and
> using the memory enable signal to enable reading from and writing to a memory. (Emphasis added.)

Applicants respectfully submit that the above recited features of Claim 7 are analogous to the previously recited features of Claim 1. Accordingly, Applicants' arguments provided above with the regard to the §103(a) rejection of Claim 1 as obvious over AAPA in view of Johnson equally apply to the §103(a) rejection of Claim 7 as obvious over such references.

Accordingly, for at least the reasons provided above, Applicants respectfully submit that the delaying of the deassertion of the clock enable signal, as taught by Johnson, for a predetermined amount of time after system activity completes or is no longer detected is provided to allow UART 108 to complete operations associated with the detected activity, as well as the completion of initialization operations. (See col. 5, lines 46-59.) In other words, Applicants respectfully submit that Johnson teaches that the immediate deassertion of the clock

enable signal, once system activity completes or is no longer detected, prohibits the UART 108 from completing operations associated with the detected activity, as well as certain initialization operations.

As a result, Johnson teaches that the deassertion of the clock enable signal for a predetermined amount of time to enable the UART 108 to complete operations associated with a detected activity as well as initialization operations. Applicants respectfully submit that the delaying of the deassertion of the clock enable signal to allow the UART 108 to complete operations associated with detected activities, as well as initialization operations, provides no teaching or teachings or suggestions with regard to the preferred latency versus power savings tradeoff which is used to set the wait period of the variable memory enable signal deassertion, as recited by Claim 7.

Accordingly, Applicants respectfully submit that the Examiner fails to establish a prima facie case of obviousness of Claim 7 since in the prior art combination of AAPA in view of Johnson fails to teach or suggest the set of a variable memory enable deassertion (MEDD) wait period based on preferred latency or a powers savings tradeoff, as recited by Claim 7. Id.

Therefore, for at least the reasons provided above, Applicants respectfully submit that Claim 7, as well dependent Claims 8-10, based on their dependencies form Claim 7, are patentable over the prior art combination of AAPA in view of Johnson. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 7-10.

Regarding Claim 11, Claim 11 recites the following claim feature which is neither taught not suggested by the prior art combination of AAPA in view of Johnson:

> the variable duration CKE signal to be asserted for access to the memory, the variable duration CKE signal set based on a preferred latency versus power savings tradeoff. (Emphasis added.)

Applicants respectfully submit that the above recited feature of Claim 11 is analogous to the previously recited features of Claims 1 and 7. Accordingly, Applicants' arguments provided

above with regard to the §103(a) rejection of Claims 1 and 7 are equally applicable to the §103(a) rejection of Claim 11 as obvious over the prior art combination of AAPA in view of Johnson.

Accordingly, for at least the reasons provided above, Applicants respectfully submit that the Examiner fails to establish a prima facie case of obviousness of Claim 11 since the prior art combination of AAPA in view of Johnson fails to teach or suggest all claim features recited by Claim 11; namely, that the variable duration CKE signal is set based on a preferred latency versus power savings tradeoff. Id.

Therefore, for at least the reasons provided above, Applicants respectfully submit that Claim 11, as well as dependent Claims 12-16, based on their dependencies from Claim 11, are patentable over the prior art combination of AAPA in view of Johnson. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 11-16.

Regarding Claim 17, Claim 17, as amended, recites the following claim feature which is neither taught or suggested by the prior art combination of AAPA in view of Johnson:

> a programmable means for setting a delay before returning the memory to the stand-by status, the delay set based on preferred latency versus power savings tradeoff. (Emphasis added.)

Applicants respectfully submit that the above recited feature of Claim 17 is analogous to the previously recited claims features of Claims 1, 7 and 11. Accordingly, Applicants' argument provided above with regard to the §103(a) rejection of Claims 1, 7 and 11 equally applied to the §103(a) rejection of Claim 17 as obvious over the prior art combination of AAPA in view of Johnson.

For at least the reasons provided above, Applicants respectfully submit that the predetermined delay for deassertion of the clock enable signal after system activity completes or is no longer detected, as taught by Johnson, is not based on a preferred latency versus power savings tradeoff, as recited by Claim 17. In contrast, the duration of the predetermined delay, as taught by Johnson, is based on the amount of time required for the UART 108 to complete operations associated with detected activity or to allow completion of initialization operations.

In contrast to Claim 17, the predetermined amount of time for delaying deassertion of the clock enable signal following completion of system activity or lack of detection of such activity is required to enable proper operation of UART 108 which may not complete operation associated with detected activity or initialization operations if the clock enable signal is immediately following the absence or the completion of the detected activity.

Accordingly, for at least the reasons provided above, Applicants respectfully submit that Applicants' amendment to Claim 17 prohibits the Examiner from establishing a prima facie case of obviousness of Claim 17 over the prior art combination of AAPA in view of Johnson since such prior art combination fails to teach or suggest the amended claim features of Claim 17. Id.

Therefore, Applicants respectfully submit that Claim 17, as well as dependent Claims 18 and 19, based on their dependencies from Claim 17, are patentable over the prior art combination of AAPA in view of Johnson. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 17-19.

Regarding Claim 20, Claim 20, as amended, recites the following claim feature which is neither taught or suggested by the prior art combination of AAPA in view of Johnson:

> a memory enable deassertion delay (MEDD) logic to set the programmable register to set a wait period for the deassertion of a memory enable signal after completion of a memory operation, the wait period chosen for a preferred latency versus power savings tradeoff. (Emphasis added.)

Applicants respectfully submit that the above recited claim feature of amended Claim 20 is analogous to the memory enable deassertion delay (MEDD) logic recited by Claim 1. Accordingly, Applicants' argument provided above with regard to the §103(a) rejection of Claim 1 equally applied to the Examiner's §103(a) rejection of Claim 20 as obvious over the prior art combination of AAPA in view of Johnson. Therefore, Applicants respectfully submit that Applicants' amendment to Claim 20 prohibits the Examiner from establishing a prima facie case of obviousness of Claim 20 since the prior art combination of AAPA in view of Johnson, for at least the reasons provided above, fails to teach or suggest that the wait period for deassertion of the memory enable signal after completion of a memory operation is chosen for a preferred latency versus power savings tradeoff, as recited by amended Claim 20. Id.

Consequently, for at least the reasons provided above, Claim 20, as well as dependent Claims 21 and 22, based on their dependencies from Claim 20, are patentable over the prior art combination of AAPA in view of Johnson. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 20-22.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: November 2, 2006

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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage on the date shown below, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Annie McNally — 11/02/2006
Annie McNally — Date